What is claimed is:

1. A microelectronic structure, comprising:

a substrate having a top surface that defines a first plane;

a dielectric disposed superjacent the top surface of the substrate;

a gate electrode disposed superjacent the dielectric, the gate electrode having first side wall spacers disposed along opposing vertical walls thereof;

a source terminal and a drain terminal each disposed, each substantially adjacent one of the first side wall spacers, partially within the substrate and partially above the substrate, the source and drain terminals further having a portion that extends laterally so as to be subjacent at least a portion of the side wall spacers;

wherein the source and drain terminals have top surfaces that define a second plane, the second plane being above the first plane, and the source and drain terminals comprise a doped crystalline semiconductor.

2. The structure of Claim 1, further comprising:

a body, disposed within the substrate, having a first portion and a second portion;

wherein the first portion is of a first conductivity type and a first doping profile, the second portion is of the first conductivity type and a second doping profile, and a transition between the first doping profile and the second doping profile is abrupt.

3. The structure of Claim 2, wherein the first portion includes counterdopants and the second portion is substantially free of counterdopants.

4. The structure of Claim 1, wherein the gate electrode comprises polysilicon disposed over the gate dielectric; and crystalline silicon of a first conductivity type disposed over the polysilicon.

5. The structure of Claim 4, wherein the gate electrode further comprises a crystalline silicon of a second conductivity type.

6. The structure of Claim 1, further comprising second side wall spacers adjacent the first side wall spacers; and metal salicide disposed in an upper portion of the gate electrode and an upper portion of the source/drain terminals.

7. The structure of Claim 6, wherein the source/drain terminals comprise p-type silicon.

8. The structure of Claim 6, wherein the source/drain terminals comprise n-type silicon.

9. The structure of Claim 6, wherein the source/drain terminals comprise p-type silicon germanium.

10. The structure of Claim 6, wherein the source/drain terminals comprise n-type silicon germanium.

11. A method of making a junction, comprising:

a) forming a patterned structure on a surface of a substrate, the substrate being of a first conductivity type;

b) isotropically etching the substrate such that a recess in the substrate is formed, the recess including a portion that underlies the patterned structure, the recess having a surface; and

c) selectively forming a layer of a first material having a second conductivity type in the recess.

12. The method of Claim 11, further comprising, prior to selectively forming the layer of the first material, selectively forming a layer of a second material having the first conductivity type over the surface of the recess.

13. The method of Claim 12, wherein the substrate comprises silicon doped to have the first conductivity type; the first material comprises doped silicon, and the second material comprises doped silicon.

14. The method of Claim 12, wherein the substrate comprises silicon doped to have the first conductivity type; the first material comprises doped silicon germanium, and the second material comprises doped silicon germanium.

15. The method of Claim 14, wherein the second material has a thickness that is less than a thickness of the first material.

16. The method of Claim 15, wherein the first material has a top surface that is above a plane defined by the surface of the substrate.

17. The method of Claim 11, wherein the patterned structure comprises a dielectric layer and a conductive material disposed over the dielectric layer.

18. The method of Claim 11, wherein etching passivates the surface of the recess.

19. The method of Claim 11, wherein etching comprises exposing the substrate to SF_6 and He in an RF plasma etching system.

20. The method of Claim 11, wherein forming the first material comprises epitaxially depositing a layer of crystalline material.

21. The method of Claim 11, wherein forming the first material comprises epitaxially depositing a layer of crystalline material; and forming the second material comprises epitaxially depositing a layer of crystalline material; wherein the substrate remains unexposed to the atmosphere subsequent to forming the first material and prior to forming the second material.

22. A method of making a transistor, comprising:

forming a dielectric on a first surface of a wafer;

forming a conductive layer overlying the dielectric;

patterning the conductive layer and dielectric so as to form a gate structure;

forming recesses adjacent and partially subjacent the gate structure; and

in a continuous operation, back filling the recesses with doped crystalline material;

wherein back filling comprises forming crystalline material of at least a first conductivity type.

23. The method of Claim 22, wherein the crystalline material of the first conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium.

24. The method of Claim 22, wherein back filling further comprises forming crystalline material of a second conductivity type.

25. The method of Claim 22, wherein the crystalline material of the second conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium.

26. The method of Claim 25, wherein back filling comprises a selective deposition.

27. A method of fabricating a FET, comprising:

forming a gate electrode having side walls over a gate insulator on a surface of a semiconductor substrate having a first conductivity type;

forming first spacers along the sidewalls of the gate electrode;

forming a recess that extends vertically down into the substrate and extends laterally through the substrate so as to underlie a portion of the gate electrode, the recess having a substrate surface;

substantially filling the recess with a fist layer of doped crystalline material, the first layer having a second conductivity type.

28. The method of Claim 27, further comprising depositing the first layer of doped crystalline material until a vertical distance between a top surface of the first layer and the surface of the substrate is greater than a vertical distance between a top surface of the gate insulator and the surface of the substrate.

29. The method of Claim 27, further comprising forming a second layer of doped crystalline material over the substrate surface of the recess, the second layer having the same conductivity type as the semiconductor substrate, and the second layer having a doping concentration that is greater than a doping concentration of the semiconductor substrate near the substrate surface of the recess.

30. The method of Claim 29, wherein forming a recess comprises placing the substrate in a parallel plate reaction chamber with a gap of approximately 1.1 cm, an RF power in the range of

approximately 50 W to 200 W, a pressure greater than approximately 500 mT, and plasma etching with sulfur hexafluoride and helium.